

IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1-30. (Canceled)

31. (Previously Presented) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses; and
a plurality of contiguous mesas comprising a plurality of contiguous top surfaces forming a
maze-like structure.

32. (Currently amended) The storage poly of claim 31, wherein ~~said~~the mesas extend
in the X, Y and Z coordinates.

33. (Currently amended) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses;
a plurality of contiguous webs comprising a plurality of contiguous top surfaces forming a maze-
like structure; and
hemispherical-grain polysilicon on at least some of ~~said~~the plurality of contiguous top surfaces.

34. (Currently amended) The storage poly of claim 33, wherein ~~said~~the webs extend
in the X, Y and Z coordinates.

35. (Currently amended) An intermediate semiconductor capacitor structure,
comprising:
a storage poly structure comprising a plurality of contiguous mesas with recesses therebetween;

a contiguous hemispherical-grain polysilicon layer on ~~said~~the storage poly structure and in contact therewith; and

a mask over ~~said~~the hemispherical-grain polysilicon layer, ~~said~~the recesses being exposed through ~~said~~the contiguous hemispherical-grain polysilicon layer and ~~said~~the mask.

36. (Canceled)

37. (Currently amended) An intermediate semiconductor memory cell structure, comprising:

a storage poly structure;

a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer on ~~said~~the storage poly structure;

recesses formed in ~~said~~the storage poly structure and located laterally between ~~said~~the plurality of contiguous low elevation regions of ~~said~~the hemispherical-grain polysilicon layer; and dielectric material at least lining the recesses.

38. (Currently amended) A semiconductor memory cell structure, comprising:
a storage poly structure;

regions of hemispherical-grain polysilicon on at least portions of an upper surface of ~~said~~the storage poly structure;

a plurality of recesses extending into ~~said~~the storage poly structure, at least some recesses of ~~said~~the plurality of recesses being located laterally between ~~said~~the regions of hemispherical-grain polysilicon and imparting the storage poly structure with a structure resembling a plurality of contiguous mesas; and

and a dielectric layer substantially coating an upper surface of ~~said~~the storage poly structure and substantially lining each of ~~said~~the plurality of recesses.

39. (Currently amended) The semiconductor memory cell structure of claim 38, further comprising a cell poly structure over ~~said~~the dielectric layer.

40. (Currently amended) The semiconductor memory cell structure of claim 38, wherein ~~said storage poly structure comprises~~ the regions of hemispherical-grain polysilicon have a web-like structure comprising a plurality of contiguous top surfaces appearance.

41. (Currently amended) The semiconductor memory cell structure of claim 38, wherein at least some of ~~said~~the plurality of recesses extend into ~~said~~the storage poly structure.

42. (Currently amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure;
a substantially confluent hemispherical-grain polysilicon layer on ~~said~~the storage poly structure;
and
a mask positioned over ~~said~~the substantially confluent hemispherical-grain polysilicon layer, ~~elevated-planarized~~ portions of ~~said~~the hemispherical-grain polysilicon layer being exposed through ~~said~~the mask.

43. (Currently amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure including recesses therein;
remaining portions of a hemispherical-grain polysilicon layer having a web-like appearance and substantially overlying upper portions of ~~said~~the storage poly structure; and
a mask positioned over ~~said~~the hemispherical-grain polysilicon layer, laterally between ~~said~~the recesses, and substantially spaced apart from ~~said~~the storage poly structure by ~~said~~the remaining portions of ~~said~~the hemispherical-grain polysilicon layer, ~~said~~the recesses in ~~said~~the storage poly structure being exposed through ~~said~~the mask.

44. (Currently amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure with recesses therein;
a hemispherical-grain polysilicon layer having a web-like appearance on at least portions of the storage poly structure; and
dielectric material lining at least ~~said~~the recesses.

45. (Currently amended) An intermediate semiconductor memory cell structure, comprising:
a storage poly structure with recesses therein;
low elevation regions of a hemispherical-grain polysilicon layer having a web-like appearance on at least portions of the storage poly structure; and
dielectric material at least lining ~~said~~the recesses.